Comparison Of Seven Level Inverter With Reduced Number Of Switches And Their Thd's In PI Controller

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Abstract—*This paper gives a description about a seven level inverter, which henceforth shows the comparison of their THD levels while comparing it with various numbers of switches. In addition to that a PI controller is simulated with RL and IM as its loads with their corresponding THD's are simulated in Matlab. The above mentioned comparison is implemented using time-domain simulation studies.*

Keywards— *PI-Proportional Integral controller, THD-Total Harmonic Distortion, HVDC- High voltage DC transmission, CSI- current source inverter, VSI-voltage source inverter, MLI - Multilevel Inverter, CHB-cascaded H bridge inverter, FCI-Flying capacitor inverter, DCI-Diode clamped inverter*.

I. INTRODUCTION

Now a day's MLI has been greatly focused to the Industrial and Grid, since MLI have investigated in the field of modular multi-level inverters have led to successful operation in HVDC systems. In recent times, in the power transmission era, for very long distances, HVDC lines based on CSI and VSI are found to be offering more economical and cost effective power transmission. But, recently HVDC transmission systems based on VSI have received increasing attention due to the many opportunities like the grid access of weak AC networks, independent control of active and reactive power, supply of passive networks and black start capability, high dynamic performance and small space requirements.

Switching power converters are used in industrial application to convert and deliver their required energy to the motor or load because of advances in solid state power devices and microprocessors .

This paper is organized into four sections. Section-1 describes the various structures of MLI. Section -II discusses the different PWM with reduced number of switches . Section III implemented in seven-level in the RL load with PI controller, and Model Predictive Controller using MATLAB / Simulink Section IV the conclusion is drawn.

The MLI are structured into three different types based on diodes, capacitors and power semiconductor devices: A) Diode clamped inverter (DCI), B) Flying capacitor inverter (FCI)   and   C) Cascaded H bridge inverter (CHB).

A. Diode clamped Inverter

The most commonly used MLI topology is DCI in which the diode is used as the clamping device to clamp the DC bus voltage so as to achieve steps in the output voltage as discussed in [1] and [4]. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is *Vdc*. A n level inverter needs (n-1) voltage sources, 2 (n-1) switching devices and (n-1) (n-2) diodes.

Figure.1 (a) shows three-level diode-clamped converter in which the DC bus has two capacitors C_1, C_2. For DC-bus voltage V_{dc}, the voltage across each capacitor is Vdc/2 and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping diodes. The staircase voltage is synthesized, the neutral point *n* is considered as the output phase voltage reference point there are three switch combinations to synthesize three-level voltages across a and n.

1. Voltage level Van= Vdc/2, turn on the switches $S_1$and S_2.
2. Voltage level Van= 0, turn on the switches S_2 and $S_{1'}$.
3. Voltage level Van= - Vdc/2 turn on the switches $S_{1'}$, $S_{2'}$.

Figure.1(b) shows a seven-level diode-clamped converter in which the DC bus consists of four capacitors C_1, C_2, C_3, and C_4. For DC-bus voltage Vdc, the voltage across each capacitor is Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes.
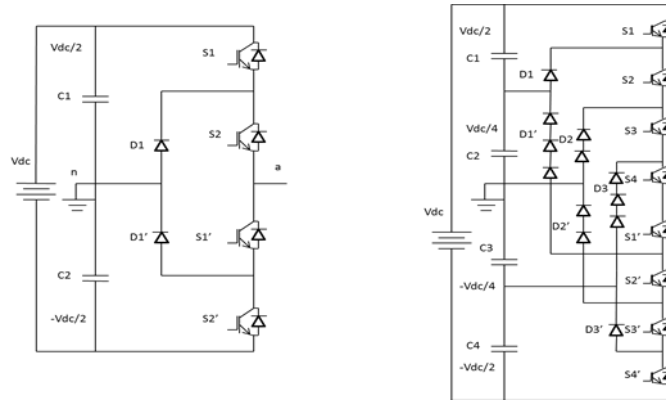
Figure.1: Diode-Clamped Multilevel Inverter Circuit Topologies.
(A) Three-Level.(B) Five-Level.

B. Flying Capacitor multilevel Inverter

The structure of Flying capacitor MLI is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter utilizes capacitors in their place. The Multicarrier PWM was explained in Flying capacitor structures which has a series connection of cells [6]. This topology has a ladder structure of dark side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Fig shows single phase n-level configuration of the capacitor clamped inverter. A *n*-level inverter will require a total of (n-1) ×(n-2) /2 clamping capacitors per phase leg in addition to (*n*-1) main DC bus capacitors. The voltage levels and the arrangements of the flying capacitors in the FCI structure assures that the voltage stress across each main device is same and is equal to *Vdc/(n*-1), for a *n*-level inverter. The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Figure.2(b) the voltage of the five-level phase-leg "a" output with respect to the neutral point n (i.e.Van), can be synthesized by the following switches combinations.

1. Voltage level Van= Vdc/2, turn on all upper switches
S1 - S4 .
2. Voltage level Van= Vdc/4, there are three combinations.
    A. Turn on switches S1, S2, S3 and S1′.(Van= Vdc/2 of   upper C4's - Vdc/4 of C1's).
    B. Turn on switches S2, S3, S4 and S4′.(Van= 3Vdc/4 of   upper C3's - Vdc/2 of C4's).
    C. Turn on switches S1, S3, S4 and S3′. (Van= Vdc/2 of   upper C4's - 3Vdc/4 or C3's + Vdc/2 of
upper C's).
3. Voltage level Van= 0, turn on upper switches S3, S4,   and lower switch S1′, S2′.
4. Voltage level Van= -Vdc/4, turn on upper switch S1 and lower switches S1′, S2′and S3′.
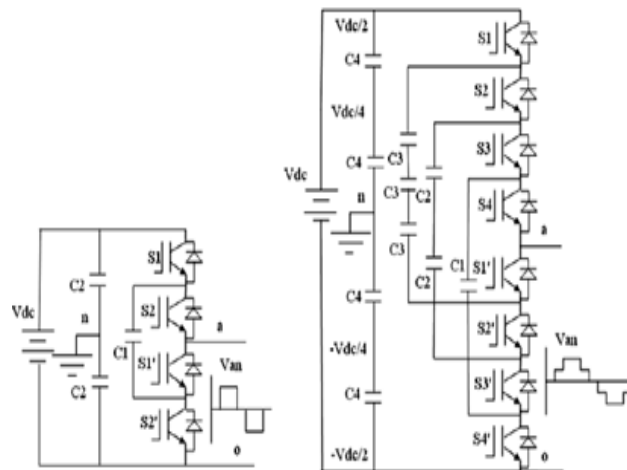5. Voltage level Van= -Vdc/2, turn on all lower switches   S1′, S2′, S3′ and S4′.

Figure.2: Capacitor-Clamped Multilevel Inverter Circuit Topologies,
(A) 3-Level Inverter (B) 5- Level Inverter.

B. Cascaded H bridge inverter

The Cascaded H bridge inverter has more advantages than other two mentioned. Cascaded H bridge inverter does not have flying capacitors and clamping diodes. The main drawback of Cascaded H bridge inverter is that the number of devices used increases with the number of levels and this increases the gate drive circuits at control stage itself causing high cost and switching losses .To overcome above disadvantages the choice is a hybrid multilevel inverter which is derived from cascaded H-bridge inverter as in [10] and [18].. In order to control the MLI output voltage there are several control techniques. The most efficient methods are based on sinusoidal PWM techniques as in [6], because it leads to easy control of inverter fundamental voltage and as well as eliminating the harmonics. These are cascaded to get the multilevel output as in [7].

For n level CHB inverter (n-1) /2 number of independent sources are required. In general independent sources may be renewable energy sources like same rated solar panels or fuel cells or wind energy sources. Single Phase Structures Of Cascaded Inverter shown in Figure.2. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of MLI is that it needs less number of components compared to the Diode clamped or the flying capacitor as in [20], so the price and the weight of the inverter is less than that of the two types.

Figure .3 shows the power circuit for one phase leg of a three-level and five-level cascaded inverter .In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive DC voltage, and negative DC voltage). This is made possible by connecting the capacitors .The resulting output AC voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc. In this topology, the number of outputs-phase voltage levels are defined by M=2N+1, where 'M' is the no of levels and 'N' is the number of DC sources. So, for an example the output phase voltage of eleven level inverter is given by
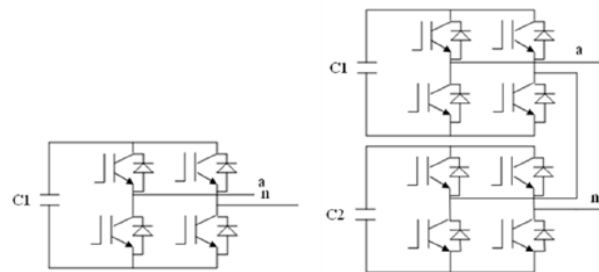
Van= Va1+Va2+Va3+Va4+Va5.

Figure.3: Single Phase Structures Of Cascaded Inverter
(A) 3-Level, (B)5-Level

II. DIFFERENT PWM WITH REDUCED NUMBER OF SWITCHES

The most efficient method of controlling output voltage is to incorporate PWM control within inverters as described in [3] and [8]. In this method, a fixed DC voltage is supplied to inverter and a controlled AC output voltage is obtained by adjusting on-off period of inverter devices. Pulse Width Modulation variable speed drives are increasingly applied in many new industrial applications that require superior performance. Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations, namely PWM inverters have become popular and considerable interested by researcher are given to them. A number of Pulse width modulation (PWM) schemes are used to obtain variable voltage and frequency supply. The most widely used PWM scheme for voltage source inverters as in [12], is sinusoidal PWM.

The control of IM number as in [16], of Pulse width modulation (PWM) schemes are used for variable voltage and frequency supply and main objective of this paper is an analysis of an Induction motor with SVPWM fed inverter and harmonic analysis of voltages & current. There is an increasing trend of using space vector PWM (SVPWM) because of it reduces the harmonic content in voltage, Increase fundamental output voltage by 15% & smooth control of IM. A space vector PWM technique is also developed based on the vector space decomposition. The techniques developed in this paper can be generalized for the control of an induction machine with an arbitrary number of phases. In space vector PWM method for a three-level inverter fed induction motor drive, a number of Pulse Width Modulation (PWM) schemes are used to obtain variable voltage and frequency supply from an inverter. There is an increasing trend of using SVPWM because of their easier digital realization and better DC bus utilization.

A. Pulse Width Modulation Technique

Because of advances in solid state power devices and microprocessors, switching power converters are used in industrial application to convert and deliver their required energy to the motor or load. PWM signals, pulse trains with fixed frequency and magnitude and variable pulse width as in [14]. There is one pulse of fixed magnitude in every PWM period. However, the width of the pulse changes from pulse to pulse according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it causes the turn on and turns off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal. The frequency of a PWM signal must be much higher than that of the modulating signal, the fundamental frequency, such that the energy delivered to the motor and its load depends mostly on the modulating signal.
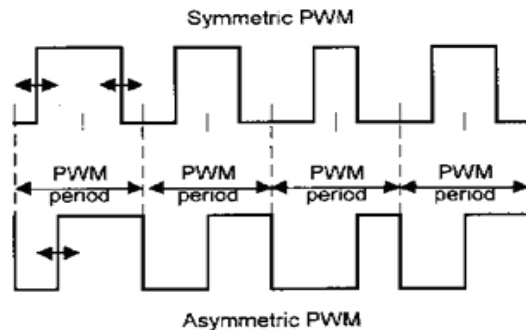

Figure 4: Symmetric and Asymmetric PWM Signals

Figure.4 shows two types of PWM signals, symmetric and asymmetric. The pulses of a symmetric PWM signal are always symmetric with respect to the center of each PWM period. The pulses of an asymmetric PWM signal always have the same side aligned with one end of each PWM period. It has been shown that symmetric PWM signals generate fewer harmonics in the output currents and voltages. This literature considers three popular PWM techniques for the most used three phase voltage source power inverter applications. This is the most popular method of controlling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control.

The advantages possessed by PWM techniques are Lower power dissipation, Easy to implement and control, No temperature variation and aging-caused drifting or degradation in linearity, Compatible with today's digital micro-processors, the output voltage control can be obtained without any additional components and with the method, lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized. The main disadvantage of this method is that SCRs are expensive as they must possess low turn-on and turn-off times.

B Single pulse width modulation

In single pulse-width modulation control, there is only one pulse per half-cycle and the width of the pulse is varied to control the output voltage. Figure 5 shows the generation of gating signals of single pulse width modulation. The gating signals are generated by:
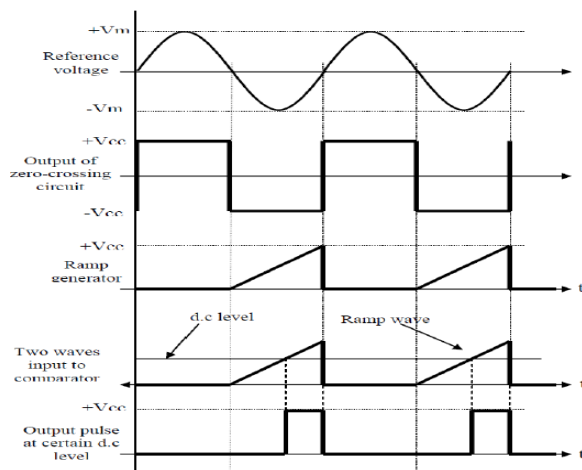

Figure 5: The generation of gating signals of single pulse width modulation

The single pulse-width modulation converts the reference signal to the square wave signal. This process is obtained by inter the reference signal to the zero-crossing circuit which considers the positive part of the input signal is positive part of the output signal(square wave) and the negative part of the input signal is negative part of the output signal as shown in Figure 5.

C Multi-Pulse width modulation

The harmonic content can be reduced by using several pulses in each half-cycle of output voltage. The generation of gating signals for turning on and off transistors is shown in Figure 6. The gating signals are produced by comparing a reference signal with a triangular carrier wave. The frequency of the reference signal sets the output frequency (fo) and carrier frequency (fc) determines the number of pulses per half cycle,

$$p = fc/2f0$$
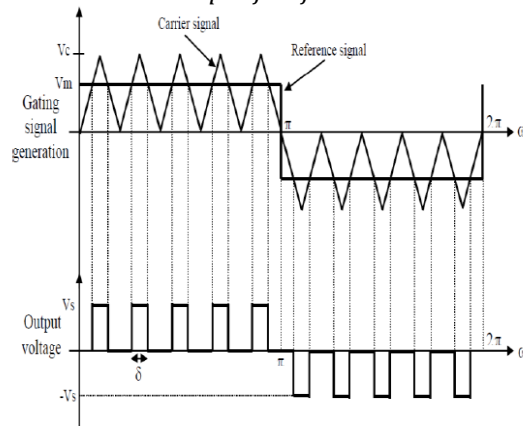
Figure 6: The generation of gating signals of multi -pulse width modulation

D The Carrier-Based Pulse Width Modulation (PWM) Technique

As mentioned earlier, it is desired that the AC output voltage Vo=VaN follow a given waveform (e.g., sinusoidal) on a continuous basis by properly switching the power valves. The carrier-based PWM technique fulfills such a requirement as it defines the on and off states of the switches of one leg of a VSI by comparing a modulating signal Vc (desired AC output voltage) and a triangular waveform VΔ (the carrier signal). In practice, when Vc > VΔ the switch S+ is on and the switch S- is off; similarly, when Vc < VΔ the switch S+ is off and the switch S- is on.
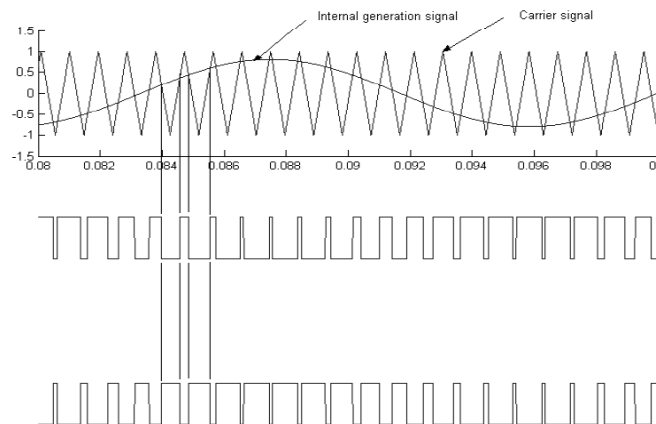
Figure 7: The generation of gating signals of Carrier-Based pulse width modulation

Figure 7 clearly shows that the AC output voltage Vo=VaN is basically a sinusoidal waveform plus harmonics. A special case is when the modulating signal Vc is a sinusoidal at frequency fc and amplitude, Ṽc and the triangular signal VΔ is are being at frequency $f\Delta$ and amplitude, ṼΔ. This is the Sinusoidal PWM (SPWM) scheme. In this case, the modulation index ma (also known as the amplitude-modulation ratio) is defined as;

$$ma = V c /V \Delta$$

And the normalized carrier frequency mf (also known as the frequency-modulation ratio) is

$$mf = f\Delta/ fc$$

III. SIMULATION RESULTS

A   Simulation study without controller

Here the simulation studies are carried under time-domain basis. We can use algorithm and direct method for pulse generation.

For simulation purposes we can use any type of switches like MOSFET,IGBT., etc. Or any other forms, the MOSFET are mostly preferable. Here an algorithm is carried out for pulse generation and also direct pulses are also given to the corresponding switches. The Figure.8 shows that it consists of twelve switches to obtain a seven level output. Here a sorting algorithm is used to decide which switch has to be turned ON and OFF correspondingly with their modulation indices. Basically here basically we use R or RL load through which we obtain the output. Both the current and voltage waveforms are measured and a sample is shown below. From the obtained output the THD is calculated and shown in the below figure. The obtained THD for twelve switches, seven level inverter is 9.00% as shown in Figure .9.
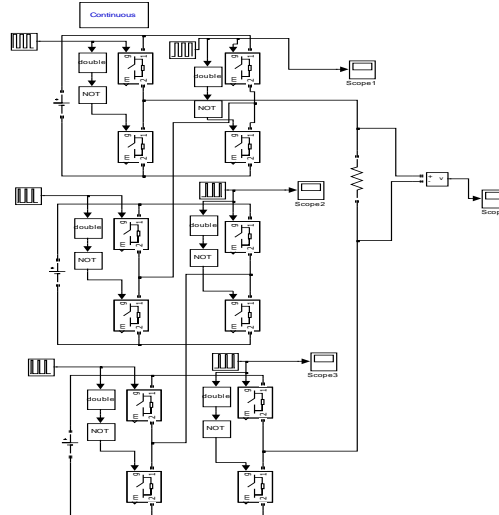

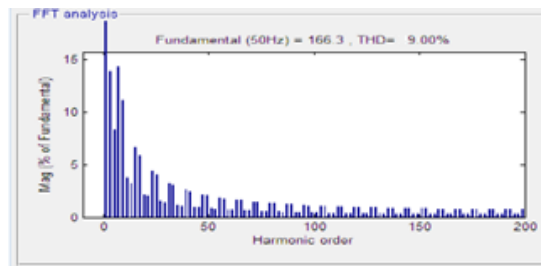Figure .8: Single phase seven level inverter with twelve switches

Figure .9: THD waveform for twelve switches(THD=9.00%)

The simulation for seven level inverter consisting of ten switches is shown in Figure.10. This structure consists of ten switches which are connected in a Cascaded H bridge manner, since it has the higher priority. The first switch conducts for positive half cycle and a second switch conducts for the negative half cycle. The sample of the waveform is shown in Figure.16 and the THD is shown in Figure.11. The THD obtained here is 7.12%
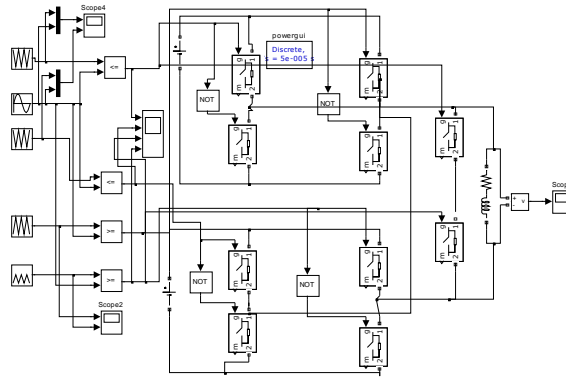
Figure .10:Single phase seven level inverter with ten switches
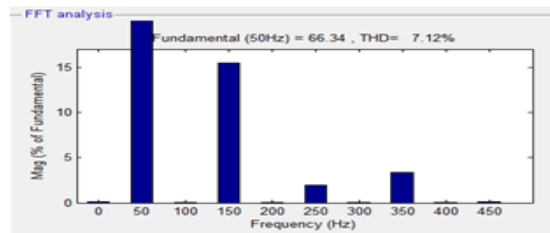

Figure .11: THD waveform for ten switches(THD=7.12%)

The simulation for seven level inverter consisting of eight switches is shown in Figure.12. It consists of eight switches which are connected in a Cascaded H bridge manner, since it has the higher priority. In the separated bridges the first bridge conducts for positive half cycle and second bridge conducts for the negative half cycle. The sample of the waveform is shown in Figure.16 and their corresponding THD is shown in Figure.13. The THD obtained here is 6.66%
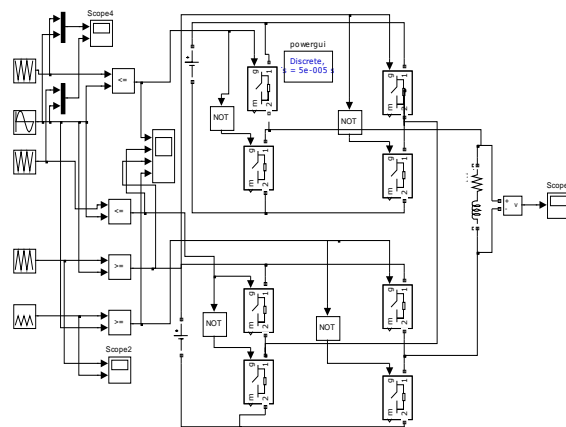

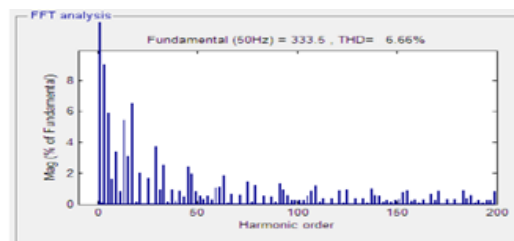Figure .12:Single phase seven level inverter with eight switches

Figure.13: THD waveform for eight switches (THD=6.66%)

The simulation for seven level inverter consisting of five switches is shown in Figure.14. It consists of five switches which are connected in a Cascaded H bridge manner. Each set of switches consists of individual pulse production. Here sorting algorithm is used to produce pulses. This construction shows a complete view of the Cascaded Multi level Inverter. Like this manner we can build n number of H bridges for various levels to obtain various THD's. The sample of the waveform is shown in Figure.16, which gives the output voltage and current waveforms for seven level inverter and their corresponding THD is shown in Figure.15. The THD obtained here is 4.15%
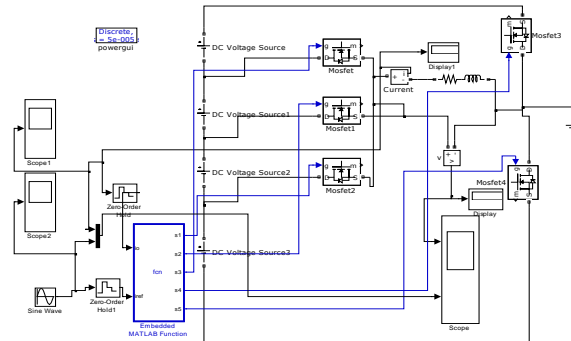

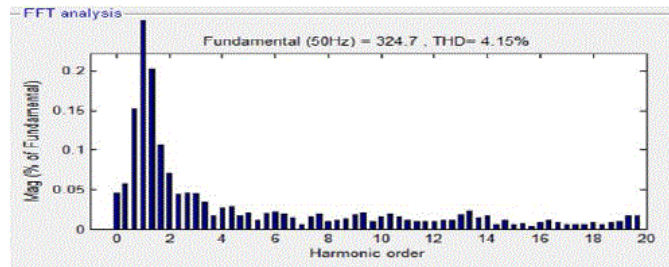Figure.14:Single phase seven level inverter with the five switches

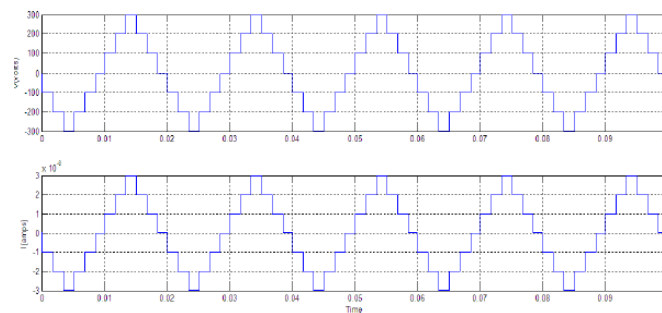Figure .15:THD waveform for five switches(THD=4.15%)

Figure .16: Output Voltage and Current waveforms for seven level inverter

B   Simulation study with controller (PI controller)

In this section the comparison is carried out in a closed loop manner, i.e., a controller is introduced. It can be any type of controller, here we are using a PI controller. The number of switches used here is five switches, their gate signals are given by means of sorting algorithm as shown in Figure 13. The load used here is a RL load and their corresponding references are fed to the controller and through the controller it is fed to the algorithm from which gate signals are generated and fed to the inverter switches. The output voltage and current waveforms are shown in Figure 18 and their corresponding THD obtained here are 16.00% as shown in Figure 14. The THD is done in MATLAB by using the FFT analysis to obtain is a particular value.
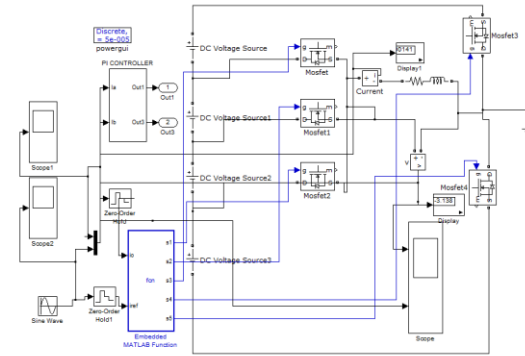
Figure 13: Single phase simulation of seven level inverter with PI controller and RL load
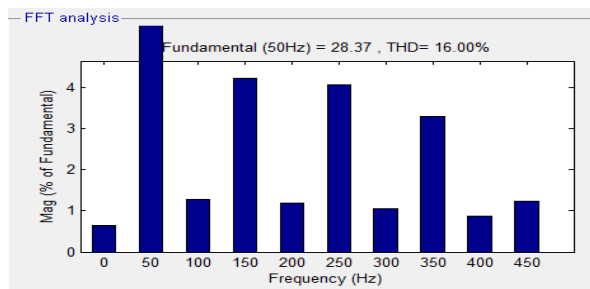

Figure .14:THD waveform (THD=16.00%)

In the second half of the system consists of same PI controller with IM as its load .Here also the same five switches are used, but only the load alone is varied .The IM used here is a normal asynchronous IM through which the following measurements are carried out: rotor current, main winding current, auxiliary winding current, rotor speed, electromagnetic torque. The same controller is fetched to the algorithm and through which pulses are fed to switches as shown in Figure 15. Their corresponding THD waveform is shown in Figure 16. The THD obtained here is 17.12%. The output waveform from the IM is also shown with their separate currents as shown in Figure 17. The output voltage and current waveforms of a seven level inverter is also shown in Figure 18.
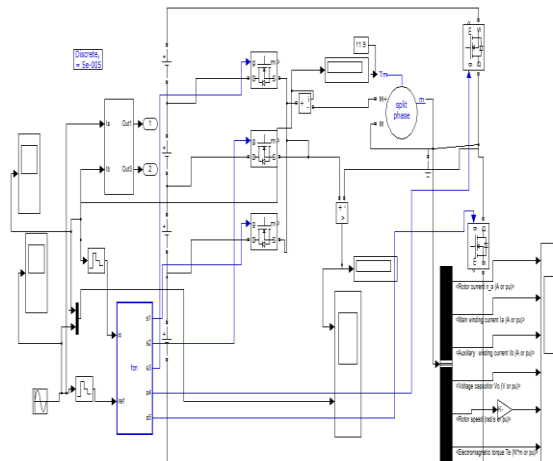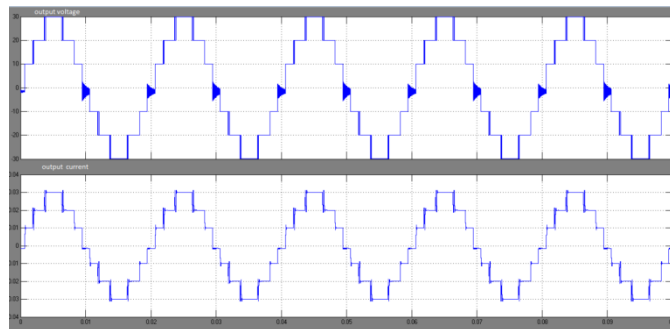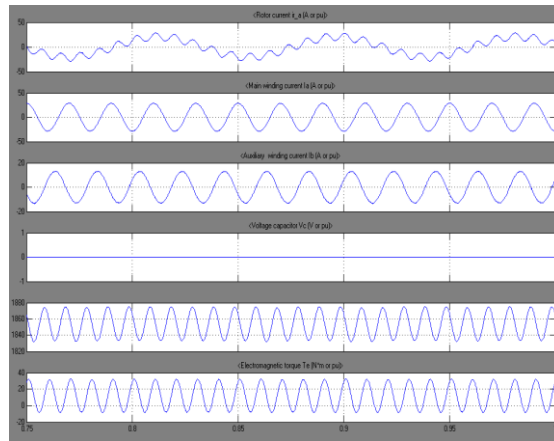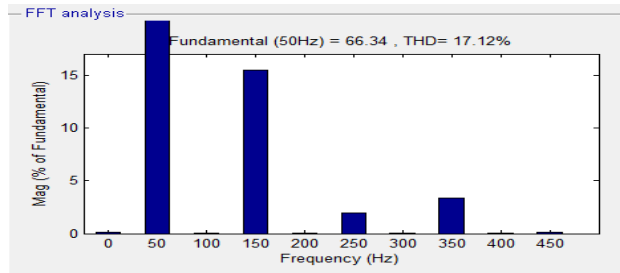

Figure 15: Single phase simulation of seven level inverter with PI controller and IM load

Figure .16: THD waveform (THD=17.12%)

Figure 17: Output waveform of IM

Figure 18: Output current and voltage waveform for seven level inverter

. Table I   Comparison of THD

SWITCHES	LEVEL	THD
12	7	9.00%
10	7	7.12%
8	7	6.66%
5	7	4.15%

IV.   CONCLUSION

The most efficient method of controlling output voltage is to incorporate PWM control within inverters. In this method, a fixed d.c. voltage is supplied to inverter and a controlled a.c. output voltage is obtained by adjusting on-off period of inverter devices with Pulse Width Modulation that require superior performance. There are so many techniques which are used for controlling of induction motor drives and PWM technique improves the quality of the current and reduce the torque ripple in induction motor drive efficiently while maintaining the other performance characteristics of the system. Table 1 shows the THD with seven level with reduced number of switches and lower switches has 4.15%

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